ASYNCHRONOUS SYSTEM-ON-A-CHIP INTERCONNECT

ABSTRACT OF THE DISCLOSURE

5   Methods and apparatus are described relating to a system-on-a-chip which includes a

plurality of synchronous modules, each synchronous module having an associated clock

domain characterized by a data rate, the data rates comprising a plurality of different data

rates. The system-on-a-chip also includes a plurality of clock domain converters. Each

clock domain converter is coupled to a corresponding one of the synchronous modules, and

10   is operable to convert data between the clock domain of the corresponding synchronous

module and an asynchronous domain characterized by transmission of data according to an

asynchronous handshake protocol. An asynchronous crossbar is coupled to the plurality of

clock domain converters, and is operable in the asynchronous domain to implement a first-

in-first-out (FIFO) channel between any two of the clock domain converters, thereby

15   facilitating communication between any two of the synchronous modules.